

REMARKS / ARGUMENTS

Claims 3-5 and 10-12 remain pending in this application. No claims have been canceled or added.

Priority

Applicants appreciate the Examiner's acknowledgment of the claim for priority and safe receipt of the priority document.

35 U.S.C. § 103

Claims 3-5 and 10-12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Bruckert et al (U.S. Patent No. 6,226,317) and Fukasawa et al (U.S. Patent No. 5,463,660) and further in view of Sawahashi et al (U.S. Patent No. 6,137,788). These rejections are traversed as follows.

The Examiner has withdrawn the indicated allowability of claims 3-5 and 10-12 in view of a newly discovered reference to Sawahashi et al. Applicants traverse this rejection based upon the deficiencies of Fukasawa which had been previously been set forth. In particular, Fukasawa simply does not disclose a single memory used for interference cancellation as in the present invention.

In an Office Action mailed January 25, 2005, the Examiner states that Fukasawa discloses a method of canceling a received signal from a base station from stored received signals and includes a method for storing received signals from

first and second base stations into a storing circuit (shift register 6) (see Office Action of January 25, 2005, page 3, line 18 to page 4, line 7). In addition, in this cited portion of the Office Action, the Examiner also alleges that Fukasawa uses a single memory (shift register 6), which is overwritten multiple times rather than using multiple memory units to iteratively cancel interference. Applicants respectfully disagree.

Fukasawa aims to improve the reception of signals received from multiple stations by repeatedly (K times) evaluating the interference from a designated station and canceling such interference. The evaluation of the interference caused by a signal from a station (i) is performed when an end of a block from station (i) is detected. The evaluated interference is canceled from the stored signals for all other stations (see Figs. 2 and 3 and column 6, lines 4-9). Since each register (each being for a station, respectively) stores K blocks (see column 3, lines 16-63) and the oldest block (K-th block) is output to the output port 19 (see column 5, lines 30-38), the block used for outputting information to the output port has had interference cancellation performed thereon a number of times (namely, $K \times (\text{number of stations} - 1)$). After repeating the evaluation, the K-th block of the register (i) has ideally only the signal from station (i), with the interference from all other stations removed.

Therefore, it should be clear that there needs to be a separate register for each of the stations (i.e., with M registers, M stations can be demodulated). Thus, when register (i) is read out and the interference caused by station (i) is evaluated, the interference is not subtracted from register (i) but from all other registers.

Therefore, Fukasawa does not disclose storing received signals from first and second base stations into a storing circuit and subtracting the replica from the storage signals and overriding the signals stored in the storing circuit. This is because the registers for reading from and overwriting to are different registers in Fukasawa. Therefore, Fukasawa does not disclose any single memory (storing circuit) as presently claimed. As such, it is submitted that the pending claims patentably define the present invention over Fukasawa.

Request for Interview

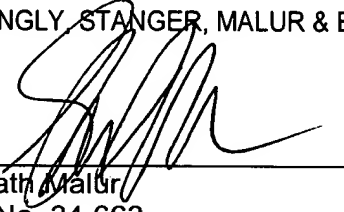
Applicants request that the Examiner conduct an interview with the undersigned in order to expedite prosecution of the present application. In this regard, the Examiner is hereby invited to contact the undersigned by telephone to arrange an appropriate time for the interview.

Conclusion

In view of the foregoing, Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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